IN CLAIMS

1-28 (Cancelled).

29. (New) A laminated chip element comprising a plurality of unit elements, comprising:

at least two sheets laminated on each other, each of the sheets having a desired property;

a plurality of first internal electrodes formed on at least one of the sheets, each of the first internal electrodes being arranged in each of the unit elements;

a second internal electrode formed on at least another of the sheets to extend over the unit elements;

a plurality of element patterns including resistors or inductors formed on the sheets, each of the element patterns being arranged in each of the unit elements;

a plurality of first and second external terminals, which are input and output terminals connected to the plurality of the first internal electrodes and to the plurality of the element patterns, respectively;

a third external terminal, which is a common terminal connected to the second internal electrode; and

a protective insulation layer formed on the uppermost one of the laminated sheets.

30. (New) The laminated chip element according to claim 29, wherein said first internal electrode includes a plurality of pairs of first and second conductive patterns formed on one of the sheets, each pair of the first and second conductive patterns being spaced apart from each other and formed at both ends of the one sheet and arranged in each of the unit elements, one ends of the first and second conductive patterns being connected to the first and second external terminals, respectively; and said second internal electrode includes a third conductive pattern formed on the other of the sheets to extend over the unit elements in a transverse direction of both the ends of the one sheet.

31. (New) The laminated chip element according to claim 29, further comprising a fourth external terminal, which is a common terminal, wherein said first internal electrode

includes a plurality of pairs of first and second conductive patterns on one of the sheets, each pair of the first and second conductive patterns being spaced apart from each other and formed at both ends of the one sheet and arranged in each of the unit elements, one ends of the first and second conductive patterns being connected to the first and second external terminals, respectively; said second internal electrode includes a third conductive pattern consisting of first and second portions which are formed on the other of the sheets to be spaced apart from each other and to extend over the unit elements in a transverse direction of both the ends of the one sheet; and both opposite ends of the first and second portions of the third conductive pattern are connected to the third and fourth external terminals, respectively.

32. (New) The laminated chip element according to claim 29, wherein said first internal electrode includes a plurality of first conductive patterns formed on one of the sheets in a direction of both ends of the one sheet, each of the first conductive patterns being arranged in each of the unit elements, and a plurality of second conductive patterns formed on another of the sheets in the same direction as the first conductive patterns, each of the second conductive patterns being arranged in each of the unit elements; both opposite ends of the first and second conductive patterns are connected to the first and second external terminals, respectively; said second internal electrode includes a third conductive pattern formed on the other of the sheets to extend over the unit elements in a transverse direction of both the ends of the one sheet; and the third conductive pattern is interposed between the first and second conductive patterns.

33. (New) The laminated chip element according to claim 29, further comprising a fourth external terminal, which is a common terminal, wherein said first internal electrode includes a plurality of first conductive patterns formed on one of the sheets in a direction of both ends of the one sheet, each of the first conductive patterns being arranged in each of the unit elements, and a plurality of second conductive patterns formed on another of the sheets in the same direction as the first conductive patterns, each of the second conductive patterns being arranged in each of the unit elements; both opposite ends of the first and second conductive patterns are connected to the first and second external terminals, respectively; said second internal electrode includes a third conductive pattern formed on a third of the sheets to extend over the unit elements in a transverse direction of both the ends of the one sheet and a fourth

conductive pattern formed on the other of the sheets to extend over the unit elements in the transverse direction of both the ends of the one sheet; both opposite ends of the third and fourth conductive patterns are connected to the third and fourth external terminals, respectively; and the third and fourth conductive patterns are interposed between the first and second conductive patterns.

34. (New) The laminated chip element according to claim 29, wherein said first internal electrode includes a plurality of first conductive patterns formed on one of the sheets in a direction of both ends of the one sheet, each of the first conductive patterns being arranged in each of the unit elements, and a plurality of second conductive patterns formed on another of the sheets in the same direction as the first conductive patterns, each of the second conductive patterns being arranged in each of the unit elements; both opposite ends of the first and second conductive patterns are connected to the first and second external terminals, respectively; said second internal electrode includes a third conductive pattern comprising a plurality of first portions formed on the other of the sheets in the same direction as the first conductive patterns and a second portion connected to one ends of the first portions, each of the first portions being arranged in each of the unit elements, the second portion being formed to extend over the unit elements in a transverse direction of both the ends of the one sheet; one end of the second portion of the third conductive pattern is connected to the third external terminal; and the third conductive pattern is interposed between the first and second conductive patterns.

35. (New) The laminated chip element according to claim 29, wherein a plurality of first conductive patterns are formed one of the sheets, each of the first conductive patterns consisting of first to third portions, the first and second portions being spaced apart from each other and formed at both ends of the one sheet, each pair of the first and second portions arranged in each of the unit elements, the third portion being spaced apart from the first and second portions and formed to extend over the unit elements in a transverse direction of both the ends of the one sheet; a plurality of second conductive patterns are formed the other of the sheets, each of the second conductive patterns consisting of fourth and fifth portions spaced from each other, the fourth portion partially overlapping with the first and third portions, the fifth portion partially overlapping with the second and third portions, each of the second conductive

patterns being arranged in each of the unit elements; said first internal electrodes comprise the first and second portions of the first conductive patterns and the second conductive patterns; said second internal electrodes comprise the third portions of the first conductive patterns; one ends of the first and second portions are connected to the first and second external terminals, respectively; one end of the third portion is connected to the third external terminal.

36. (New) The laminated chip element according to any one of claim 29, wherein areas of overlapping portions between the internal electrodes differ from each other.

37. (New) The laminated chip element according to any one of claim 29, wherein metal pads are formed to be spaced apart from each other, and the element pattern is formed to connect the metal pads to each other.

38. (New) The laminated chip element according to any one of claim 29, wherein the protective insulation layer includes epoxy or glass.

39. (New) The laminated chip element according to any one of claim 29, wherein the element patterns include inductive patterns, some of the inductive patterns of the unit elements are formed on an upper surface of the laminated chip element, and the other of the inductive patterns of the unit elements are formed on a lower surface of the laminated chip element.

40. (New) The laminated chip element according to any one of claim 29, wherein the element pattern includes an inductive pattern, the inductive pattern is spiral, an insulated bridge is formed in a radial direction across the spiral inductive pattern, and a bridge pattern for extending a central end of the inductive pattern to an outside thereof is formed on the insulated bridge.

41. (New) The laminated chip element according to any one of claim 29, wherein the element pattern includes an inductive pattern, a ferrite layer is form on the laminated chip element, and the inductive pattern is formed on the ferrite layer.

42. (New) The laminated chip element according to any one of claim 29, wherein the element pattern includes resistive material, such as Ni-Cr, RuO_2.

43. (New) The laminated chip element according to any one of claim 29, wherein the element patterns include inductive patterns, a plurality of inductor sheets are further laminated, at least one of the inductive patterns are formed on each of the inductor sheets, and both ends of the respective inductive patterns are connected to the corresponding first and second external terminals.

44. (New) The laminated chip element according to any one of claim 29, wherein the element patterns include inductive patterns, a plurality of inductor sheets are further laminated, an inductive pattern is formed on each of the inductor sheets, the inductive patterns are connected to each other in series through through-holes formed in the inductor sheets, both ends of the connected inductive patterns are connected to the first and second external terminals, respectively.